

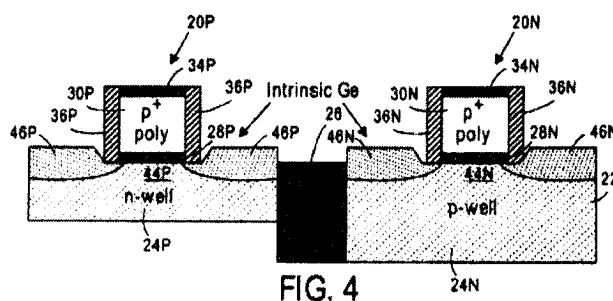
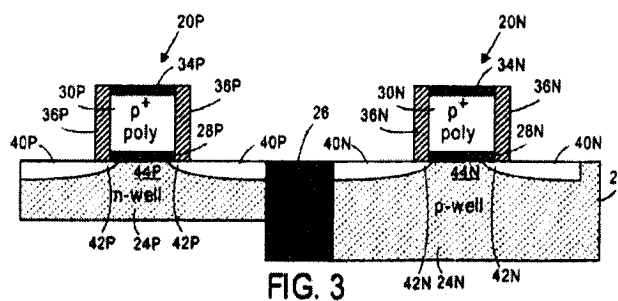
REMARKS

Claims 1-49 were previously pending in the present application. No claims are currently canceled or added. Consequently, claims 1-49 remain pending. Reconsideration of the present application in light of the following remarks is respectfully requested.

Rejections under 35 U.S.C. §102

Claim 1

Claims 1 and 11 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. App. No. 2005/0079660 to Murthy, et al. ("Murthy"). Claim 1 requires an NMOS or PMOS device that includes source/drain regions that are recessed within the substrate surface. The Examiner rejects claim 1 stating "wherein a first one of the NMOS and PMOS devices 20N/20P includes first source/drain regions 46N/P recessed within the surface (see Fig. 3 and par. [0030])." Examiner's Office Action, page 2. In contrast, while the source/drain regions 46 N/P of Murthy are formed in corresponding recesses 40N/P, and the source/drain regions 46 N/P actually extend above the substrate surface, as shown in Murthy's Figs. 3 and 4 set forth below.



It is clear from the above figures of Murthy that the source/drain regions 46 N/P of Murthy are not recessed within the substrate surface in the context of claim 1 of the present application. That is, the top surfaces of the source/drain regions 46 N/P are all “higher” than the surface of the substrate 22. The source/drain regions 46 N/P each extend above the substrate 22. None of the source/drain regions 46 N/P are recessed within the substrate 22 in the context of claim 1 of the present application because the source/drain regions 46 N/P each protrude from the substrate 22.

Moreover, even if the source/drain regions 46 N/P were considered to be recessed within the substrate 22 in the context of claim 1 of the present application (which, as described above, is clearly not true), then Murthy would necessarily fail to disclose additional source/drain regions which extend above the substrate 22. That is, the source/drain regions 46P of the PMOS device 20P are shaped identical to the source/drain regions 46N of the NMOS device 20N. Consequently, if the source/drain regions 46P of the PMOS device 20P are “recessed within” the substrate 22, as alleged by the Examiner, then the source/drain regions 46N of the NMOS device 20N must necessarily also be recessed within the substrate 22 and, thus, cannot extend above the substrate 22 in the context of claim 1 of the present application. However, this is clearly not the case because, as shown in Fig. 4, the source/drain regions of both the NMOS and PMOS devices 20 N/P extend above the substrate.

Therefore, the §102 rejection of claim 1 is not supported by Murthy. Accordingly, Applicants respectfully request that the Examiner withdraw the §102 rejection of claim 1 and its dependent claim 11.

Claim 44

Claim 44 is also rejected under 35 U.S.C. §102(e) as being anticipated by Murthy. However, claim 44 requires an NMOS or PMOS device that includes source/drain regions that are recessed within the substrate surface. As described above, Murthy fails to provide such

disclosure. Therefore, the §102 rejection of claim 44 is not supported by Murthy. Accordingly, Applicants respectfully request that the Examiner withdraw the §102 rejection of claim 44.

Rejections under 35 U.S.C. §103: Murthy in view of Bohr

Claims 5-9, 12, and 15, which each depend from claim 1, are rejected under 35 U.S.C. §103(a) as being unpatentable over Murthy in view of U.S. Pat. App. No. 2004/0262683 to Bohr, et al. ("Bohr"). Applicants traverse this rejection on the grounds that these references are defective in establishing a *prima facie* case of obviousness with respect to claim 1.

As described above, Murthy fails to teach NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 1 of the present application. Moreover, Bohr fails to cure this shortcoming of Murthy because Bohr also fails to teach one device having source/drain regions recessed within the substrate and another device having source/drain regions extending above the substrate, in the context of claim 1 of the present application.

Moreover, neither Murthy nor Bohr suggests forming NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 1 of the present application. That is, Murthy and Bohr each teach source/drain regions which are either coplanar with the substrate or which extend from the substrate, but neither reference teaches, suggests, or even hints at the source/drain regions of one of the devices being recessed within the substrate while the source/drain regions of the other one of the devices extend above the substrate.

Therefore, even when combined, Murthy and Bohr fail to teach or suggest each and every element of claim 1 of the present application. Consequently, the combination of Murthy and Bohr fails to support a *prima facie* case of obviousness of claim 1 and its dependent claims.

Accordingly, Applicants respectfully request that the Examiner withdraw the §103 rejection of claims 5-9, 12, and 15.

Rejections under 35 U.S.C. §103: Murthy in view of Bohr and Dawson

Claim 1

Claims 2-4, 13, and 14, which depend from claim 1, are rejected under 35 U.S.C. §103(a) as being unpatentable over Murthy in view of Bohr and further in view of U.S. Pat. No. 5,963,803 to Dawson, et al. ("Dawson"). Applicants traverse this rejection on the grounds that these references are defective in establishing a *prima facie* case of obviousness with respect to claim 1.

As described above, whether taken separately or together, Murthy and Bohr fail to teach NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 1 of the present application. Moreover, Dawson fails to cure this shortcoming of Murthy and Bohr because Dawson also fails to teach one device having source/drain regions recessed within the substrate and another device having source/drain regions extending above the substrate, in the context of claim 1 of the present application.

Moreover, Murthy, Bohr, and Dawson each fail to suggest forming NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 1 of the present application. That is, Murthy, Bohr, and Dawson each teach source/drain regions which are either coplanar with the substrate or which extend from the substrate, but none of the references teaches, suggests, or even hints at the source/drain regions of one of the devices being recessed within the substrate while the source/drain regions of the other one of the devices extend above the substrate.

Therefore, even when combined, Murthy, Bohr, and Dawson fail to teach or suggest each and every element of claim 1 of the present application. Consequently, the combination of

Murthy, Bohr, and Dawson fails to support a *prima facie* case of obviousness of claim 1 and its dependent claims. Accordingly, Applicants respectfully request that the Examiner withdraw the §103 rejection of claims 2-4, 13, and 14.

Claim 16

Claims 16-22 and 24-27 are also rejected under 35 U.S.C. §103(a) as being unpatentable over Murthy in view of Bohr and further in view of Dawson. Applicants traverse this rejection on the grounds that these references are defective in establishing a *prima facie* case of obviousness with respect to claim 16.

Claim 16 requires NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate. However, as described above, Murthy, Bohr, and Dawson collectively fail to teach or suggest NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 16 of the present application.

Therefore, even when combined, Murthy, Bohr, and Dawson fail to teach or suggest each and every element of claim 16 of the present application. Consequently, the combination of Murthy, Bohr, and Dawson fails to support a *prima facie* case of obviousness of claim 16 and its dependent claims. Accordingly, Applicants respectfully request that the Examiner withdraw the §103 rejection of claims 16-22 and 24-27.

Claim 28

Claims 28-33 and 35-37 are also rejected under 35 U.S.C. §103(a) as being unpatentable over Murthy in view of Bohr and further in view of Dawson. Applicants traverse this rejection on the grounds that these references are defective in establishing a *prima facie* case of obviousness with respect to claim 28.

Claim 28 requires NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate. However, as described above, Murthy, Bohr, and Dawson collectively fail to teach or suggest NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 28 of the present application.

Therefore, even when combined, Murthy, Bohr, and Dawson fail to teach or suggest each and every element of claim 28 of the present application. Consequently, the combination of Murthy, Bohr, and Dawson fails to support a *prima facie* case of obviousness of claim 28 and its dependent claims. Accordingly, Applicants respectfully request that the Examiner withdraw the §103 rejection of claims 28-33 and 35-37.

Claim 44

Claims 45 and 46, which depend from claim 44, are also rejected under 35 U.S.C. §103(a) as being unpatentable over Murthy in view of Bohr and further in view of Dawson. Applicants traverse this rejection on the grounds that these references are defective in establishing a *prima facie* case of obviousness with respect to claim 44.

Claim 44 requires NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate. However, as described above, Murthy, Bohr, and Dawson collectively fail to teach or suggest NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 44 of the present application.

Therefore, even when combined, Murthy, Bohr, and Dawson fail to teach or suggest each and every element of claim 44 of the present application. Consequently, the combination of Murthy, Bohr, and Dawson fails to support a *prima facie* case of obviousness of claim 44 and its

dependent claims. Accordingly, Applicants respectfully request that the Examiner withdraw the §103 rejection of claims 45 and 46.

Rejections under 35 U.S.C. §103: Murthy in view of Bohr and Biebl

Claim 1

Claim 10, which depends from claim 1, is rejected under 35 U.S.C. §103(a) as being unpatentable over Murthy in view of Bohr and further in view of U.S. Pat. No. 5,913,115 to Biebl, et al. (“Biebl”). Applicants traverse this rejection on the grounds that these references are defective in establishing a *prima facie* case of obviousness with respect to claim 1.

As described above, whether taken separately or together, Murthy and Bohr fail to teach NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 1 of the present application. Moreover, Biebl fails to cure this shortcoming of Murthy and Bohr because Biebl also fails to teach one device having source/drain regions recessed within the substrate and another device having source/drain regions extending above the substrate, in the context of claim 1 of the present application.

Moreover, Murthy, Bohr, and Biebl each fail to suggest forming NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 1 of the present application. That is, Murthy, Bohr, and Biebl each teach source/drain regions which are either coplanar with the substrate or which extend from the substrate, but none of the references teaches, suggests, or even hints at the source/drain regions of one of the devices being recessed within the substrate while the source/drain regions of the other one of the devices extend above the substrate.

Therefore, even when combined, Murthy, Bohr, and Biebl fail to teach or suggest each and every element of claim 1 of the present application. Consequently, the combination of Murthy, Bohr, and Biebl fails to support a *prima facie* case of obviousness of claim 1 and its

dependent claims. Accordingly, Applicants respectfully request that the Examiner withdraw the §103 rejection of claim 10.

Claim 16

Claim 23, which depends from claim 16, is also rejected under 35 U.S.C. §103(a) as being unpatentable over Murthy in view of Bohr and further in view of Biebl. Applicants traverse this rejection on the grounds that these references are defective in establishing a *prima facie* case of obviousness with respect to claim 16.

Claim 16 requires NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate. However, as described above, Murthy, Bohr, and Biebl collectively fail to teach or suggest NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 16 of the present application.

Therefore, even when combined, Murthy, Bohr, and Biebl fail to teach or suggest each and every element of claim 16 of the present application. Consequently, the combination of Murthy, Bohr, and Biebl fails to support a *prima facie* case of obviousness of claim 16 and its dependent claims. Accordingly, Applicants respectfully request that the Examiner withdraw the §103 rejection of claim 23.

Claim 28

Claim 34, which depends from claim 28, is also rejected under 35 U.S.C. §103(a) as being unpatentable over Murthy in view of Bohr and further in view of Biebl. Applicants traverse this rejection on the grounds that these references are defective in establishing a *prima facie* case of obviousness with respect to claim 28.

Claim 28 requires NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending

above the substrate. However, as described above, Murthy, Bohr, and Biebl collectively fail to teach or suggest NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 28 of the present application.

Therefore, even when combined, Murthy, Bohr, and Biebl fail to teach or suggest each and every element of claim 28 of the present application. Consequently, the combination of Murthy, Bohr, and Biebl fails to support a *prima facie* case of obviousness of claim 28 and its dependent claims. Accordingly, Applicants respectfully request that the Examiner withdraw the §103 rejection of claim 34.

Rejections under 35 U.S.C. §103: Murthy in view of Wu

Claim 47 is rejected under 35 U.S.C. §103(a) as being unpatentable over Murthy in view of U.S. Pat. No. 6,194,258 to Wu (“Wu”). Applicants traverse this rejection on the grounds that these references are defective in establishing a *prima facie* case of obviousness with respect to claim 47.

As described above, Murthy fails to teach NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate. Moreover, Wu fails to cure this shortcoming of Murthy because Wu also fails to teach one device having source/drain regions recessed within the substrate and another device having source/drain regions extending above the substrate.

Moreover, neither Murthy nor Wu suggests forming NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 47 of the present application. That is, Murthy and Wu each teach source/drain regions which are either coplanar with the substrate or which extend from the substrate, but neither reference teaches, suggests, or even hints at the source/drain regions of one of the devices being recessed within the substrate while the source/drain regions of the other one of the devices extend above the substrate.

Therefore, even when combined, Murthy and Wu fail to teach or suggest each and every element of claim 47 of the present application. Consequently, the combination of Murthy and Wu fails to support a *prima facie* case of obviousness of claim 47. Accordingly, Applicants respectfully request that the Examiner withdraw the §103 rejection of claim 47.

Rejections under 35 U.S.C. §103: Murthy in view of Wu and Dawson

Claims 48 and 49, which depend from claim 47, are rejected under 35 U.S.C. §103(a) as being unpatentable over Murthy in view of Wu and further in view of Dawson. Applicants traverse this rejection on the grounds that these references are defective in establishing a *prima facie* case of obviousness with respect to claim 47.

As described above, whether taken separately or together, Murthy and Wu fail to teach NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 47 of the present application. Moreover, Dawson fails to cure this shortcoming of Murthy and Wu because Dawson also fails to teach one device having source/drain regions recessed within the substrate and another device having source/drain regions extending above the substrate, in the context of claim 47 of the present application.

Moreover, Murthy, Wu, and Dawson each fail to suggest forming NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 47 of the present application. That is, Murthy, Wu, and Dawson each teach source/drain regions which are either coplanar with the substrate or which extend from the substrate, but none of the references teaches, suggests, or even hints at the source/drain regions of one of the devices being recessed within the substrate while the source/drain regions of the other one of the devices extend above the substrate.

Therefore, even when combined, Murthy, Wu, and Dawson fail to teach or suggest each and every element of claim 47 of the present application. Consequently, the combination of

Murthy, Wu, and Dawson fails to support a *prima facie* case of obviousness of claim 47 and its dependent claims. Accordingly, Applicants respectfully request that the Examiner withdraw the §103 rejection of claims 48 and 49.

Rejections under 35 U.S.C. §103: Yeo in view of Murthy

Claims 38, 39, and 42 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. App. No. 2004/0173815 to Yeo, et al. (“Yeo”) in view of Murthy. Applicants traverse this rejection on the grounds that these references are defective in establishing a *prima facie* case of obviousness with respect to claim 38.

As described above, Murthy fails to teach NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate. Moreover, Yeo fails to cure this shortcoming of Murthy because Yeo also fails to teach one device having source/drain regions recessed within the substrate and another device having source/drain regions extending above the substrate.

Moreover, neither Murthy nor Yeo suggests forming NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 38 of the present application. That is, Murthy and Yeo each teach source/drain regions which are either coplanar with the substrate or which extend from the substrate, but neither reference teaches, suggests, or even hints at the source/drain regions of one of the devices being recessed within the substrate while the source/drain regions of the other one of the devices extend above the substrate.

Therefore, even when combined, Murthy and Yeo fail to teach or suggest each and every element of claim 38 of the present application. Consequently, the combination of Murthy and Yeo fails to support a *prima facie* case of obviousness of claim 38 and its dependent claims. Accordingly, Applicants respectfully request that the Examiner withdraw the §103 rejection of claims 38, 39, and 42.

Rejections under 35 U.S.C. §103: Yeo in view of Murthy and Bohr

Claim 43, which depends from claim 38, is rejected under 35 U.S.C. §103(a) as being unpatentable over Yeo in view of Murthy and further in view of Bohr. Applicants traverse this rejection on the grounds that these references are defective in establishing a *prima facie* case of obviousness with respect to claim 38.

As described above, whether taken separately or together, Yeo, Murthy, and Bohr fail to teach or suggest NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the substrate, in the context of claim 38 of the present application. That is, Yeo, Murthy, and Bohr each teach source/drain regions which are either coplanar with the substrate or which extend from the substrate, but none of the references teaches, suggests, or even hints at the source/drain regions of one of the devices being recessed within the substrate while the source/drain regions of the other one of the devices extend above the substrate.

Therefore, even when combined, Yeo, Murthy, and Bohr fail to teach or suggest each and every element of claim 38 of the present application. Consequently, the combination of Yeo, Murthy, and Bohr fails to support a *prima facie* case of obviousness of claim 38 and its dependent claims. Accordingly, Applicants respectfully request that the Examiner withdraw the §103 rejection of claim 43.

Rejections under 35 U.S.C. §103: Yeo in view of Murthy and Dawson

Claims 40 and 41, which depend from claim 38, are rejected under 35 U.S.C. §103(a) as being unpatentable over Yeo in view of Murthy and further in view of Dawson. Applicants traverse this rejection on the grounds that these references are defective in establishing a *prima facie* case of obviousness with respect to claim 38.

As described above, whether taken separately or together, Yeo, Murthy, and Dawson fail to teach or suggest NMOS and PMOS devices in which one device has source/drain regions recessed within the substrate and the other device has source/drain regions extending above the

substrate, in the context of claim 38 of the present application. That is, Yeo, Murthy, and Dawson each teach source/drain regions which are either coplanar with the substrate or which extend from the substrate, but none of the references teaches, suggests, or even hints at the source/drain regions of one of the devices being recessed within the substrate while the source/drain regions of the other one of the devices extend above the substrate.

Therefore, even when combined, Yeo, Murthy, and Dawson fail to teach or suggest each and every element of claim 38 of the present application. Consequently, the combination of Yeo, Murthy, and Dawson fails to support a *prima facie* case of obviousness of claim 38 and its dependent claims. Accordingly, Applicants respectfully request that the Examiner withdraw the §103 rejection of claims 40 and 41.

Conclusion

All matters set forth in the Office Action have been addressed. Accordingly, it is believed that all claims are in condition for allowance. Favorable consideration and an early indication of allowability are respectfully requested.

Should the Examiner deem that an interview with Applicants' undersigned attorney would expedite consideration, the Examiner is invited to call the undersigned attorney at the telephone number indicated below.

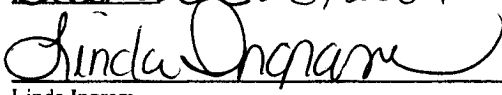
Respectfully submitted,



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I hereby certify that this correspondence is being filed with the U.S. Patent and Trademark Office via EFS-Web on <u>December 28, 2007.</u>
 Linda Ingram